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ISCT based Control of DSTATCOM in 3-phase, 4-wire System for Load Compensation

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Abstract—*Power Quality issues are the major concern in the low voltage distribution system. The paper suggests a shunt connected custom power device (DSTATCOM) to provide load compensation in the 3-phase, 4-wire network. The performance of the DSTATCOM is analyzed for two three leg VSI topologies; with single DC capacitor and with split DC capacitor under unbalanced and non-linear load. An Instantaneous Symmetrical Component Theory (ISCT) based Hysteresis Current Controller (HCC) has been introduced to generate switching pulses for VSI. A comparative analysis has been carried out for the DSTATCOM comprising of two VSI topologies on the basis of %THD and neutral current compensation. A DSTATCOM behavior using split DC capacitor topology is found to be more effective than VSI with single DC Capacitor. An extensive digital simulation is done using MATLAB/SIMULINK environment showing improved compensation performance.*

Index Terms*: Non-linear and unbalanced Load, DSTATCOM, Voltage Source Inverter (VSI), Hysteresis Current Controller, Instantaneous Symmetrical Component Theory*

1. INTRODUCTION

Good power quality means faultless power supply that has pure, noise-free and sinusoidal wave shape and is always within the voltage and frequency tolerance. Maintaining the power quality in the distribution system is a very difficult task because of increasing industrial and commercial power demand. The use of power electronics devices is increasing day by day, which leads to various power quality issues in the distribution network and thus degrading the system performance.

Power quality issues can be mainly classified into two categories: Voltage based issues and current based issues. Current based issues include current harmonics, reactive power and excessive neutral current. To compensate these issues, many devices are available such as DVR and DSTATCOM. This paper suggests the use of DSTATCOM for the mitigating the current based issues.

The main component of DSTATCOM is Voltage Source Inverter (VSI). A number of conventional VSI topologies for DSATCOM configuration are available such as Single DC capacitor VSI topology, Split DC Capacitor VSI topology and

4-leg VSI topology. Using DSTATCOM with single DC capacitor VSI topology does not compensate the neutral current. Therefore, for neutral current compensation a Split DC capacitor VSI topology is been used. This topology uses two common capacitors, with a center tap connected to the line neutral and thus providing a return path for neutral current. Four leg VSI topology can also be used to compensate neutral current as fourth leg provides return path for the neutral current with a single capacitor. However, maintaining the co-ordination between fourth leg and the other three legs of VSI becomes too complex in case of Four leg VSI.

As DSTATCOM injects current, Hysteresis Current Controller (HCC) is preferred to generate switching pulses for inverter. Hysteresis Current Controller requires reference current which is to be compared with the actual injected compensator current to generate the switching pulses. For this purpose, various reference current generation algorithms are available such as Instantaneous p-q Theory, Instantaneous Modified p-q Theory, Synchronous Reference Frame Theory, Instantaneous Symmetrical Component Theory and Vectorial Method. Among these, Instantaneous Symmetrical Component Theory (ISCT) is most preferred algorithm because of its simplicity of implementation.

This paper suggests the comparative analysis of two VSI topologies used for DSTATCOM with ISCT based Hysteresis controller. Among them split DC capacitor topology is found to be more effective for providing load compensation.

2. SYSTEM UNDER STUDY

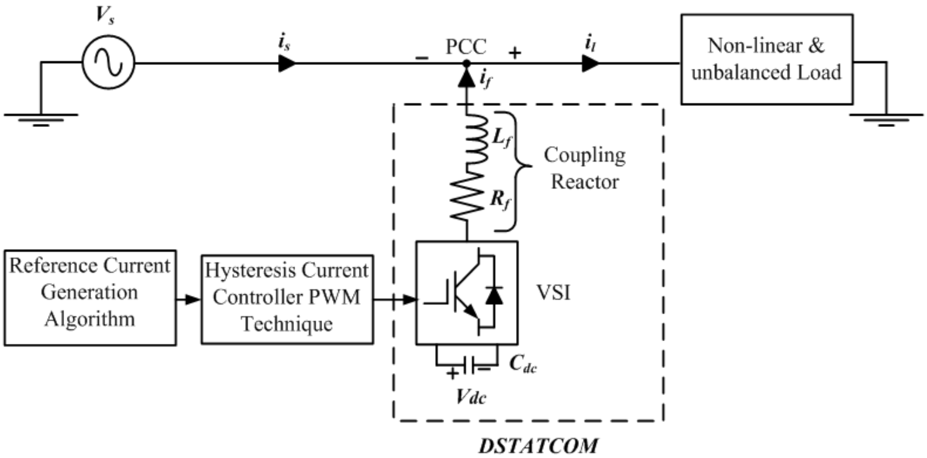

Figure 1. Single Line structure of DSTATCOM

A three phase, four wire system including a DSTATCOM configuration is shown in Fig.1.

This paper presents a distribution system with non-linear and unbalanced load. Due to non-linear and unbalanced load, current based power quality issues are generated. To mitigate these issues, a DSTATCOM is used.

The main component of DSATCOM is Voltage Source Inverter (VSI). Various topologies can be used for DSTATCOM configuration. The VSI topology is connected in shunt at the point of common coupling and through the interface reactor.

In this stiff system, the non-linearity is introduced through a rectifier load. For creating switching pulses required for VSI, Hysteresis Current Controlled PWM technique is used to trigger switches. For Hysteresis Control Method, reference currents are required which can be acquired through various algorithms available among which ISCT is implemented for reference current generation. The system parameters are given in Table 1.

Table 1: System Parameters

Supply Voltage	Supply voltage of 230 V_{rms}/ phase, 50 Hz
R-L Load	R_a = 150Ω L_a = 100mH R_b = 75Ω L_b = 100mH R_c = 50Ω L_c = 10mH
Non- Linear Load	Three phase uncontrolled rectifier with R = 300Ω, L = 100mH
Interface Inductor	R_f=1Ω, L_f=30mh
Hysteresis band	±h = 0.08 A
PI controller gains	K_p =1, K_i = 0.5
DC Voltage	V_{dc}=500V(Single DC) V_{dc1}=V_{dc}=500V(Split DC)
V_{dcref}	510 V(Single DC), 1100V(Split DC)
DC Capacitor	C_{dc}= 2200µF , Cdc1=Cdc2=2200µF

3. CONVENTIONAL VSI TOPOLOGIES FOR LOW VOLTAGE DISTRIBUTION SYSTEM

A. VSI with single DC Capacitor

Fig.2. shows VSI with Single DC Capacitor which consists of six switches (S1-S6). A control scheme is required to operate the VSI switches. This paper reveals a hysteresis current controller which has been introduced for switching operation. In this topology, DSTATCOM is connected in shunt through interface inductor at the point of common coupling (PCC).

If loads are unbalanced and non-linear, the load currents will have a zero sequence component. In this topology, there

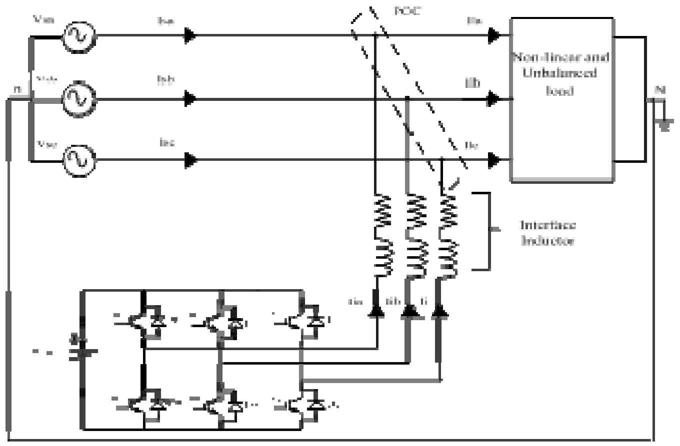

Figure 2: Single DC Capacitor VSI Topology

is no return path provided for zero sequence of the current. Therefore, this topology cannot interject the current having a zero sequence component. Full compensation is not achieved as zero sequence components are not compensated. This shows the imperfection of single DC capacitor inverter.

B.VSI with split DC Capacitor

VSI with split DC Capacitor is given in the Fig.3. The neutral of the load and the source are connected together to the neutral of the Split DC Capacitor. There will be a return path for Zero Sequence component as shown in the fig.3.i.e. path N-n. The Zero Sequence component will be compensated by the DSTATCOM as it is able to supply this component for unbalanced and non-linear load. Simulation results are predicted in fig.6.

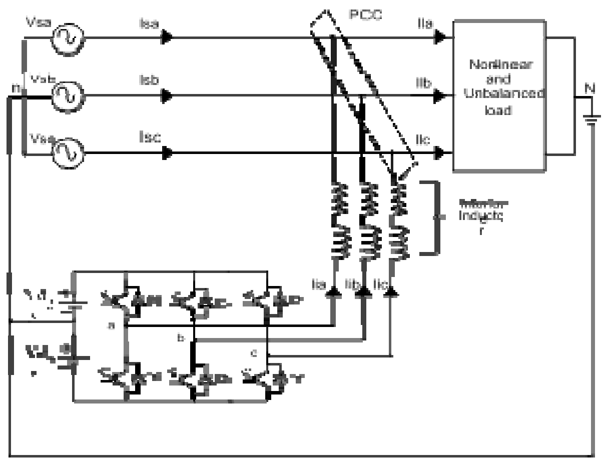

Fig.3. Split DC Capacitor VSI topology

Here, the value of DC capacitor is taken to be 2200µF for simulation purposes. The value of capacitor can be increased up to the value of 10000 µF without changing any parameters of the system except the voltage of DC Capacitor. It is selected in such a way that it will have lesser ripples. For better performance, the value of capacitor will increase in such a way that it acts like a battery and so the proportional and integral gains of PI controller will have to be increased.

4. HYSTERESIS CURRENT CONTROLLER

Hysteresis Current Controlled pulse width modulation is widely used because of its easy utilization, fast intense feedback with potential to limit peak current. This current controller is used to activate the switch of voltage source inverter. The objective of hysteresis current controller is to force the actual injected current to follow the reference quantity. It starts to track the desired reference current from the point of common coupling. The logic equation of Hysteresis Current Controller can be given by-

I act >I ref + h then -1

I act < I ref -h then +1

The difference between the desired current $i_{ref}$and the injected current I_{actual} is called the error. When error reaches the lower limit, upper switches of inverter conducts and the current is forced to increase. When error reaches the lower limit, upper switches of inverter conducts and forces the current down.

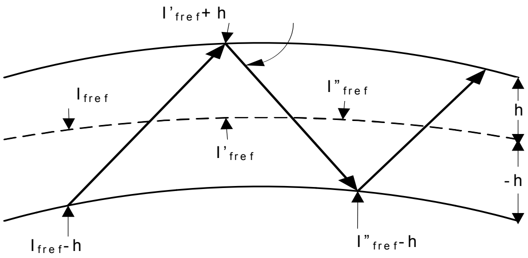

Figure 4: Hysteresis Current Controller

From Fig, 4. the dotted line represents the reference currents. The upper limit is created by adding hysteresis band to the reference currents i.e. (i_{ref}+h). The lower limit is created by subtracting hysteresis band from the reference currents (I_{ref}-h). The triangular wave depicts the actual hysteresis current. As the actual injected current exceeds the upper band i.e. (I_{ref}+h), lower switches(2, 4, 6) conducts and as it crosses the lower band, i.e.(i_{ref}-h), upper switches (1, 3, 5) are conducted.

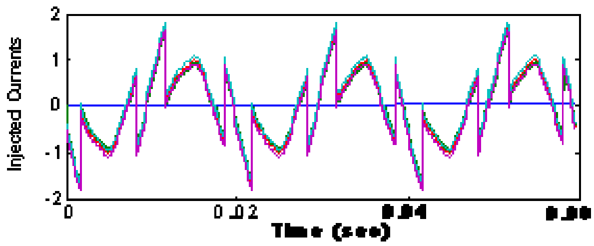

Figure.5. Hysteresis Band

Fig.5. shows that the injected current produced by DSTATCOM follows the reference current which forms a Hysteresis Band of phase a.In essence, the inverter becomes a current source with a peak to peak current ripple. The current is controlled within the hysteresis band. The switching pulses S_1, S_2, S_3, S_4, S_5 and S_6 are given to VSI to compensate the harmonic current produced by non-linear load.

5. REFERENCE CURRENT GENERATION

Mainly, the control algorithm used for the extraction of reference current components decides the performance and amount of benefits achieved by using DSTATCOM. There are various control algorithms available such as Instantaneous p-q Theory, Instantaneous Modified p-q Theory, Synchronous Reference Frame Theory, Instantaneous Symmetrical Component theory. Instantaneous p-q Theory requires transformation which increases control complexity of system.

Hence, the usage of Instantaneous Symmetrical Component Theory (ISCT) is preferred. ISCT is popular due to its easy implementation among the various control algorithms. It also does not require any transformation.

The purpose of compensation in 3-phase Four-wire system is to provide a balanced supply current in such a way that its zero sequence components are zero.

Therefore,

$$i_{Sa} + i_{Sb} + i_{Sc} = 0 \quad (1)$$

The algorithm forces this source current to be unity power factor.

By assuming that the source voltages are balanced, they can be given by-

$$\begin{aligned} v_{Sa} &= \sin \omega t \\ V_{Sb} &= \sin\left(\omega t - 120^o\right) \\ V_{Sc} &= \sin\left(\omega t + 120^o\right) \end{aligned} \quad (2)$$

From symmetrical components,

$$\begin{bmatrix} V_{a0} \\ V_{a1} \\ V_{a2} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (3)$$

Therefore, the positive sequence component of source voltage V_{sa} will be,

$$V_{Sa_1} = \frac{1}{\sqrt{3}}\left\{V_{Sa} + aV_{Sb} + a^2 V_{Sc}\right\} \quad (4)$$

(4)

Where,

$$a = e^{j120}$$

And,

$$e^{j\theta} = \cos\theta + j\sin\theta$$

Therefore,

$$\begin{aligned} e^{j120} &= \cos 120 + j\sin 120 \\ &= \frac{-1}{2} + j\frac{\sqrt{3}}{2} \end{aligned} \quad (5)$$

$$\begin{aligned} a^2 = e^{j240} &= \cos 240 + j\sin 240 \\ &= \frac{-1}{2} - j\frac{\sqrt{3}}{2} \end{aligned} \quad (6)$$

Therefore,

$$V_{Sa1} = \frac{1}{\sqrt{3}}\left\{V_{Sa} + \left(\frac{-1}{2}\right)V_{Sb} + j\frac{\sqrt{3}}{2}V_{Sb} + \left(\frac{-1}{2}\right)V_{Sc} + j\left(\frac{-\sqrt{3}}{2}\right)V_{Sc}\right\} \quad (7)$$

And as,

$$\tan\delta = \frac{\sin\delta}{\cos\delta}$$

Now, from equation (7) angle of the vector is given by,

$$\delta = \angle V_{Sa1} = \tan^{-1}\left\{\frac{\frac{\sqrt{3}}{2}V_{Sb} - \frac{\sqrt{3}}{2}V_{Sc}}{V_{Sa} - \frac{1}{2}V_{Sb} - \frac{1}{2}V_{Sc}}\right\}$$

$$\frac{k_1}{k_2} = \frac{\left(\frac{k_3}{k_4}\right) + \tan\delta}{1 - \left(\frac{k_3}{k_4}\right).\tan\delta}$$

$$\delta = \tan^{-1}\left\{ \frac{\frac{\sqrt{3}}{2}\left(V_{Sb} - V_{Sc}\right)}{\frac{3}{2}V_{Sa}} \right\} \quad (8)$$

By substituting the value of V_{sa}, V_{sb} and V_{sc}

$$\delta = \tan^{-1}\left\{ \frac{-\cos\omega t}{\sin\omega t} \right\} = \omega t - \frac{\pi}{2} \quad (9)$$

From the power factor consideration, it isassumed that the phase of the vector is zero. Current lags that Vsa1 by an angle

$$\angle\left\{V_{Sa} + aV_{Sb} + a^2V_{Sc}\right\} = \angle\left\{i_{Sa} + ai_{Sb} + a^2 i_{Sc}\right\} + \delta \quad (10)$$

By substituting the values of a and a^2in equation 3,

$$\angle\left\{\left(V_{Sa} - \frac{1}{2}V_{Sb} - \frac{1}{2}V_{Sc}\right) + j\frac{\sqrt{3}}{2}\left(V_{Sb} - V_{Sc}\right)\right\}$$

(11)

$$= \angle\left\{\left(i_{Sa} - \frac{1}{2}i_{Sb} - \frac{1}{2}i_{Sc}\right) + j\frac{\sqrt{3}}{2}\left(i_{Sb} - i_{Sc}\right)\right\} + \delta$$

After equating the angles,

$$\tan^{-1}\left(\frac{k_1}{k_2}\right) = \tan^{-1}\left(\frac{k_3}{k_4}\right) + \delta \quad (12)$$

Where, from equation

$$k_1 = \frac{\sqrt{3}}{2}\left(V_{Sb} - V_{Sc}\right) \quad (13)$$

$$k_2 = \left(V_{Sa} - \frac{1}{2}V_{Sb} - \frac{1}{2}V_{Sc}\right) \quad (14)$$

$$k_3 = \frac{\sqrt{3}}{2}\left(i_{Sb} - i_{Sc}\right) \quad (15)$$

$$k_4 = \left(i_{Sa} - \frac{1}{2}i_{Sb} - \frac{1}{2}i_{Sc}\right) \quad k_4 = \left(i_{Sa} - \frac{1}{2}i_{Sb} - \frac{1}{2}i_{Sc}\right) \quad (16)$$

Using formula,

$$\tan\left(\alpha + \beta\right) = \frac{\tan\alpha + \tan\beta}{1 - \tan\alpha.\tan\beta} \quad (17)$$

Equation (14) can be expressed as,

$$\frac{k_1}{k_2} = \tan\left[\tan^{-1}\left(\frac{k_3}{k_4}\right) + \delta\right] \quad (18)$$

Applying above formula,

$$\left(V_{Sb} - V_{Sc} - 3\beta V_{Sa}\right)i_{Sa} + \left(V_{Sc} - V_{Sa} - 3\beta V_{Sb}\right)i_{Sa} + \left(V_{Sa} - V_{Sb} - 3\beta V_{Sc}\right)i = 0 \quad (20)$$

$$\begin{bmatrix} 1 & 1 & 1 \\ V_{Sb} - V_{Sc} - 3\beta V_{Sa} & V_{Sc} - V_{Sa} - 3\beta V_{Sb} & V_{Sa} - V_{Sb} - 3\beta V_{Sc} \\ V_{Sa} & V_{Sb} & V_{Sc} \end{bmatrix} \begin{bmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ P_{l_{avg}} \end{bmatrix}$$

(19)

Putting the value of k_1 ar
above equation,
Where,

$$\beta = \frac{\tan\delta}{\sqrt{3}}$$

Here, β can be defined as the wanted fraction of average reactive power of load which is to be supplied by the Source.
When the power factor angle is assumed to be zero, equation 6 implies that the instantaneous reactive power supplied by the source is zero.

When the angle is non-zero, the source supplies the reactive power that is equal to be β times the instantaneous power.
The objective of the compensation is to supply the oscillating component such that the source supplies the average value of the load power.

$$V_{Sa}i_{Sa} + V_{Sb}i_{Sb} + V_{Sc}i_{Sc} = P_{l_{avg}} \quad (21)$$

Where, P_{lavg} is a load power obtained by feeding the instantaneous load power to a low pass filter.

$$P_{l_{avg}} = V_{Sa}.i_{Sa} + V_{Sb}.i_{Sb} + V_{Sc}.i_{Sc} \quad (22)$$

Since, the harmonic component in the load does not require any real power, the source only supplies the real power required by the load.
By combining equations (1), (20) and (21)

By applying KCL at PCC,

$$i_{refk} = i_{lk} - i_{sk} \quad (24)$$

Where k=a, b, c
Substituting above equation in equation

$$i_{a_{ref}} = i_{la} - i_{sa} \quad (23)$$

Hence, the reference compensator currents can be expressed as,

$$i_{a_{ref}} = i_{la} - \frac{V_{Sa} + (V_{Sb} - V_{Sc})\beta}{V_{Sa}^2 + V_{Sb}^2 + V_{Sc}^2} P_{l_{avg}} \quad (25)$$

Similarly,

$$i_{b_{ref}} = i_{lb} - \frac{V_{Sb} + (V_{Sc} - V_{Sa})\beta}{V_{Sa}^2 + V_{Sb}^2 + V_{Sc}^2} P_{l_{avg}} \quad (26)$$

$$i_{c_{ref}} = i_{lc} - \frac{V_{Sc} + (V_{Sa} - V_{Sb})\beta}{V_{Sa}^2 + V_{Sb}^2 + V_{Sc}^2} P_{l_{avg}} \quad (27)$$

6. SIMULATION RESULTS

a. Uncompensated system

Simulation results of three-phase four wire distribution system without connecting DSTATCOM under non-linear and unbalanced load is predicted in Fig. 6. The source voltages arebalanced and sinusoidal at both non-linear and unbalanced load in Fig. 6(a). On Unbalanced load, source currents and load currents are not in phase at time 0.03sec and after 0.03sec amplitude of both currents are different. Fig. 6(b) and Fig. 6(c) shows non-linearity and unbalancing of the waves of source currents and load currents.

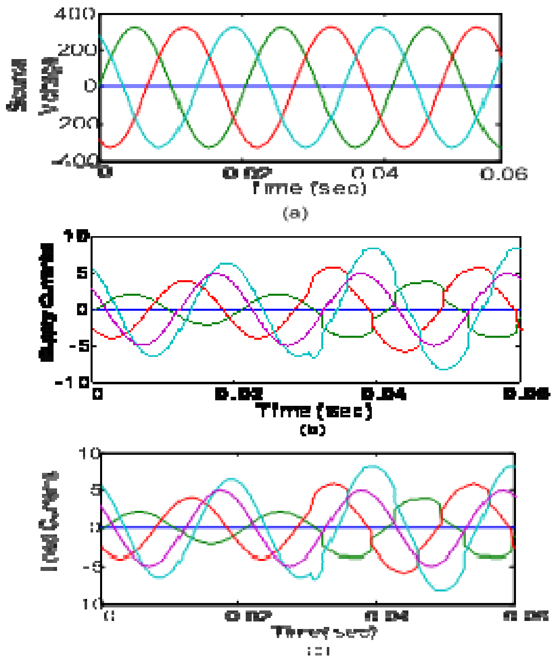

Fig.6. Uncompensated System
(a)Source Voltages (b)Source Currents (c)Load Currents

b. Compensated System

I. Reference Currents

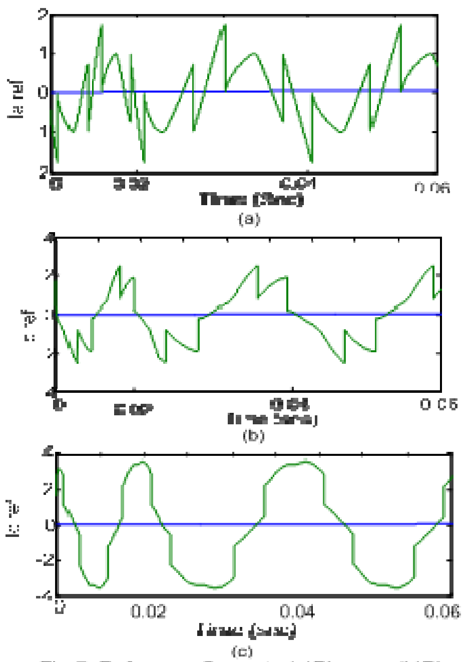

Fig.7. Reference Currents (a)Phase a (b)Phase b
(c)Phase c

Fig. 7 shows the references of phases a, b, and c produced by the Instantaneous Symmetrical Component Theory (ISCT).

II.DSTATCOM performance using VSI with single dc capacitor

The simulation results of DSTATCOM with single dc capacitor VSI under unbalanced and non-linear load are presented in Fig.8. Fig.8(c) shows load currents which are unbalanced and distorted because of unbalanced and non-

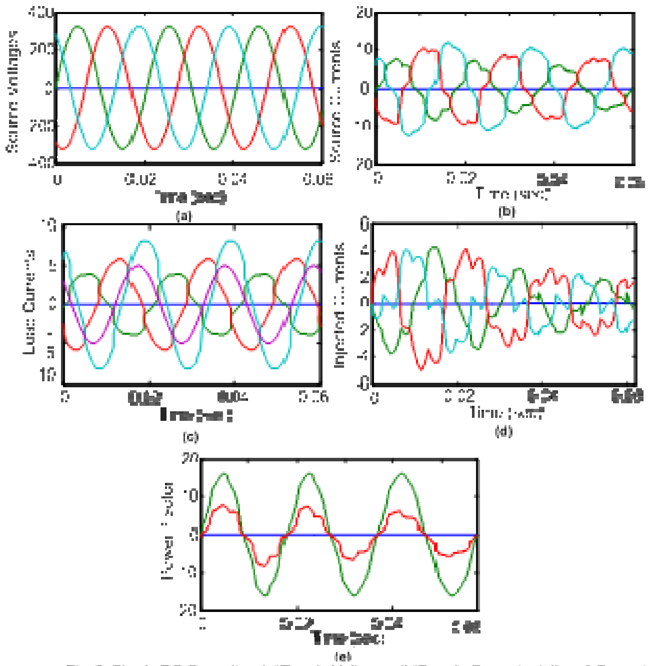

Fig. 8. Single DC Capacitor (a)Supply Voltages (b)Supply Currents (c)Load Currents (d)Injected Currents (e)Power Fcator

Table 2: Comparative Analysis

		%THD			Power Factor			Neutral Current In (A)
		Phase a	Phase b	Phase c	Phase a	Phase b	Phase c	
Uncompensated System	Single Dc Capacitor	14.9%	10.4%	7.2%	0.995	0.95	0.998	2.958
	Split DC Capacitor	14.9%	10.4%	7.2%	0.995	0.95	0.998	2.958
Compensated System	Single DC Capacitor	12.5%	11.4%	11.1%	0.999	0.987	0.998	2.958
	Split DC Capacitor	4.45%	4.41%	4.6%	1	0.99	1	0.098

linear load. The compensator injected current by DSATCOM portrayed in Fig.8 (d) tracks the reference current during compensation. From Fig.8 (b), it can be seen that due to incomplete compensation, source currents are neither balanced, nor sinusoidal. It can be deduced from Fig.8 (e) that the power factor was not able to obtain the value of unity.

This is because of unsatisfactory performance of DSTACOM and inadequacy to compensate zero sequence current. Hence, this topology gives partial compensation.

III. DSTATCOM performance using VSI split dc capacitor

From Fig. 9(d), it is seen that the reference and injected current are tracked in all the phases.Load currents are distorted and unbalanced as shown in Fig.9(c).

Source currents are balanced and sinusoidal with zero neutral current and are in phase with the corresponding Voltage Source. Thus, the value of Power Factor is unity as presented in Fig.9(e). From this simulation result, it is proved that Split DC capacitor VSI topology gives effective performance in compensation.

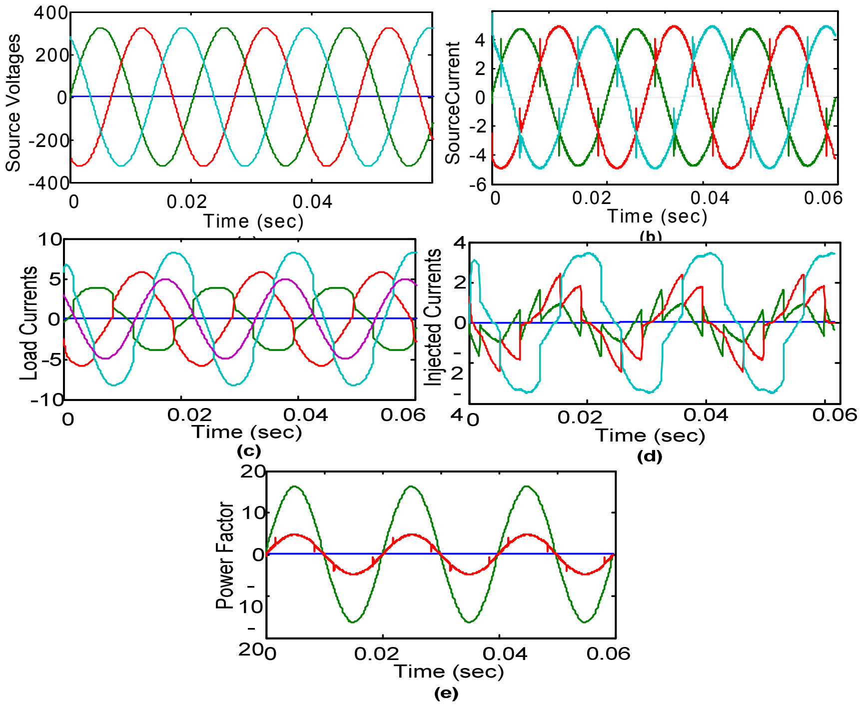

Fig.9. Split DC capacitor (a)Source Voltages (b)Source Currents (c)Load Currents (d)Injected Currents (e)Power Factor

7. CONCLUSION

This paper discusses the use of DSTATCOM for load compensation with the help of two VSI topologies. Simulation is carried out in MATLAB/SIMULINK. Incorporation of two VSI topologies shows that the split DC capacitor VSI topology is more efficient. It gives better compensation under unbalanced and non-linear load condition. To attain the better compensation performance, ISCT based hysteresis current controller is used which gives more prominent results. It is thus concluded that ISCT based hysteresis current controller with split DC capacitor VSI topology for DSTATCOM configuration is more efficient than single DC capacitor VSI topology under unbalanced and non-linear load condition.

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